BUR920010040US2 Serial No. 10/695,335

## AMENDMENTS TO THE CLAIMS

## IN THE CLAIMS:

For completeness, it is noted that claims 1-12 were cancelled in Applicants'

Preliminary Amendment of October 28, 2003. Claims 13-20 are currently pending, as hereinbelow:

13. (Currently Amended) A thin film insulating (FIN) metal oxide semiconductor field effect transistor (MOSFET) comprising:

a bottom Si-containing layer;

an insulating region present atop said bottom Si-containing layer, said insulating region having at least one partial opening therein:

a gate region formed in said partial opening, said gate region comprising two regions of gate conductor that are separated from <u>vertical</u> channel regions by an insulating film, said insulating film <u>comprising a gate dielectric and</u> having opposite vertical surfaces adjacent to the <u>vertical</u> channel regions;

source/drain diffusion regions abutting said gate region, said source/drain diffusion regions having junctions that are self-aligned to the <u>vertical channels</u> channel regions as well and the gate region; and

BUR920010040US2 Serial No. 10/695,335

insulating spacers that separate the gate region and the source/drain diffusion region regions formed orthogonal to said insulating film;

to thereby provide a double-gated/double channel MOSFET device.

- 14. (Original) The FIN MOSFET of Claim 13 wherein said insulating region includes an insulating layer of an SOI material.
- 15. (Original) The FIN MOSFET of Claim 13 wherein said partial opening exposes a portion of said insulating layer of said SOI material.
- 16. (Currently Amended) The FIN MOSFET of Claim 13 wherein said insulating film is formed surrounding a portion of a Si-containing layer, said insulating film is comprised of a gate dielectric.
- 17. (Original) The FIN MOSFET of Claim 16 wherein said gate dielectric is comprised of an oxide, a nitride, an oxynitride or any combination or multilayer thereof.

BUR920010040US2 Serial No. 10/695,335

- 18. (Original) The FIN MOSFET of Claim 13 wherein said regions of gate conductor are each comprised of polysilicon, amorphous Si, a conductive elemental metal, an alloy of a conductive elemental metal, a nitride or silicide of a conductive elemental metal or multilayers thereof.
- 19. (Original) The FIN MOSFET of Claim 13 further comprising salicide regions formed atop said source/drain diffusion regions.
- 20. (Original) The FIN MOSFET of Claim 13 wherein said source/drain diffusion regions are formed in a portion of a patterned Si-containing layer.